WHAT IS CLAIMED IS:

1. A method for estimating remaining film thickness distribution of a surface protection film that remains on each activation region after chemical mechanical polishing when a semiconductor substrate having the surface protection film is etched using a patterning mask that has a mask pattern for producing an activation region to form a device isolation trench so as to create the activation region, an insulating film is provided over the activation region to fill the device isolation trench, and chemical mechanical polishing is performed on the semiconductor substrate with the insulating film provided thereon to form a device separating portion,

the patterning mask comprising a plurality of one-chip mask regions arranged in matrix, and each of the one-chip mask regions comprising the same number of the mask patterns in the same layout,

the method for estimating remaining film thickness distribution comprising:

a step for generating a reduced region on each of the mask patterns by removing a predetermined width from the mask pattern along the edge of the mask pattern;

a step for segmentalizing the one-chip mask region into predetermined segmentalized regions to generate segmentalized regions and for acquiring an area ratio of all reduced regions with respect to each of the segmentalized regions, the all reduced regions occupying a

region that includes the segmentalized region at a fixed position and has the same size and shape as those of the one-chip mask region; and

a step for acquiring the distribution of the remaining film thickness in the one-chip mask region on the basis of the area ratio.

2. The method for estimating remaining film thickness distribution according to Claim 1, wherein the reduced region is generated so as to have substantially the same size and shape as those of a top surface region of the insulating film that covers the activation region corresponding to the reduced region.

3. A method for estimating remaining film thickness distribution of a surface protection film that remains on each activation region after chemical mechanical polishing when a semiconductor substrate having the surface protection film is etched using a patterning mask that has a mask pattern for forming an activation region to form a device isolation trench so as to create the activation region, an insulating film is provided over the activation region to fill the device isolation trench, and chemical mechanical polishing is performed on the semiconductor substrate with the insulating film provided thereon to form a device separating portion,

the patterning mask comprising a plurality of one-chip

mask regions arranged in matrix, and each of the one-chip mask regions comprising the same number of the mask patterns in the same layout,

the method for estimating remaining film thickness distribution comprising:

a step for generating a reduced region for each of the mask patterns by removing a predetermined width from each mask pattern along the edge of the mask pattern;

a step for generating a frame-shaped region by removing, from the mask pattern, a regional portion that overlaps the reduced region corresponding to the mask pattern;

a step for segmentalizing the one-chip mask region into predetermined segmentalized regions to generate segmentalized region and for acquiring an area ratios of all reduced regions and frame-shaped regions, respectively, with respect to each of the segmentalized region, the reduced regions and frame-shaped regions occupying a region that includes the segmentalized region at a fixed position and has the same size and shape as those of the one-chip mask region in each of the segmentalized regions; and

a step for acquiring the distribution of the remaining film thickness in the one-chip mask region on the basis of the area ratio of the reduced regions and the area ratio of the frame-shaped regions.

4. A patterning mask design method for designing a

patterning mask by using the method for estimating remaining film thickness distribution according to any one of Claims 1 to 3, comprising:

a step for extracting a first region predicted to have a high polishing rate in the one-chip mask region; and

a step for setting a first pseudo mask pattern for forming a first pseudo activation region outside the mask pattern in the first region.

5. The patterning mask design method according to Claim 4, further comprising:

a step for extracting a second region predicted to have a low polishing rate in the one-chip mask region; and

a step for designing a second pseudo mask pattern for forming a second pseudo activation region outside the mask pattern in the second region, wherein

a ratio of area of the mask pattern and the regions in which the first and second pseudo mask patterns are formed that occupies each one-chip mask region is substantially fixed.

6. The patterning mask design method according to Claim 5, wherein an elongate region is set as the second pseudo mask pattern in the step for forming the second pseudo mask pattern.

7. The patterning mask design method according to any

one of Claims 4 to 6, wherein the space size of the first pseudo mask pattern is set according to the space size of the region outside the mask pattern of the first region.

8. The patterning mask design method according to any one of Claims 4 to 7, wherein the area ratio of the first pseudo mask pattern occupying the area outside the mask pattern in a first region is increased according to a predicted level of polishing rate in a plurality of the first regions in the step for forming the first pseudo mask pattern.

9. A manufacturing method for a semiconductor device using the patterning mask according to any one of Claims 4 to 8, comprising:

a step for etching the semiconductor substrate having the surface protection film by using the patterning mask so as to form a left activation region and a device isolation trench produced by the etching.